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(54) Method of producing semiconductor device and semiconductor device.

(57) A method of producing a semiconductor device comprising the steps of depositing an alloy film (14) including copper (Cu) on a substrate (10,12), patterning the alloy film, and annealing the patterned alloy film in an ambient atmosphere including at least nitrogen (N_2) gas, so that a copper interconnection film (18) covered by a nitride film (16) is formed.

FIG. 1A

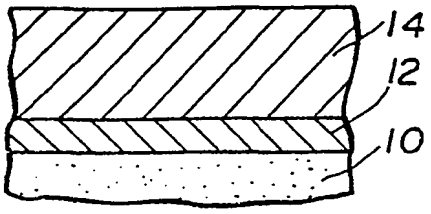


FIG. 1C

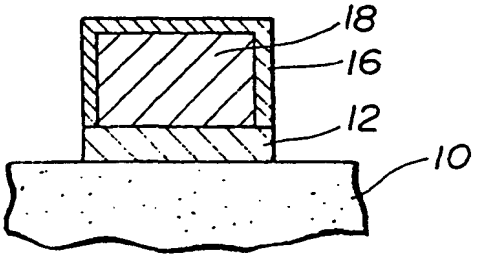
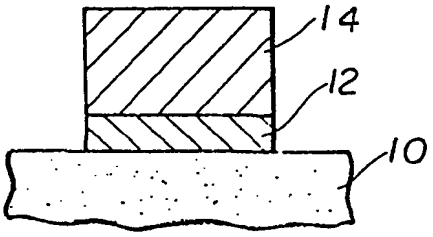


FIG. 1B



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METHOD OF PRODUCING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention generally relates to a method of producing a semiconductor device, and a semiconductor device produced by the method. The present invention more particularly relates to a method of producing a semiconductor device using copper or copper alloy as a wiring or metallization material.

As well known, a metallization pattern of a large scale integrated circuit (LSI) diminishes in width as its integration density increases. Although aluminum (Al) metallization is widely used for semiconductor chips, its width for metallization is limited to the range of 0.5 to 0.6 μm. This is because electromigration increasingly occurs as the aluminum metallization pattern becomes narrower. For this reason, use of a metallic material of a high melting point such as molybdenum (Mo) or tungsten (W) in replace of Al is considered. However, the resistivity of Mo or W is approximately twice the resistivity of Al in bulk and is more in a thin film. Therefore, a metallization material having a high electromigration resistance and a low resistivity is currently being investigated.

Presently, copper (Cu) is being investigated for metallization of LSIs due to its better electromigration resistance and lower resistivity than Al. A conventional semiconductor device with copper metallization is designed so that a copper metallization film is directly deposited on an insulating film such as silicon dioxide (SiO_2) which is deposited on a silicon (Si) substrate and over contact holes formed in the insulating film so as to be positioned on the top of diffused layers formed in the Si substrate. Of course, the copper film is patterned in accordance with the wiring pattern.

The semiconductor device thus produced is generally annealed at a high temperature of the order of 400°C or over in order to grow grains of Cu and to thereby improve the electromigration resistance. Thereafter, an insulating film is deposited on the Cu metallization film as well as the insulating film. The deposition of the insulating film is conventionally carried out by a chemical vapor deposition (CVD) at a temperature of approximately 420°C. The insulating film on the copper metallization film may be made of, for example, phosphor-silicate glass (PSG), silicon nitride (Si_3N_4) or SiO_2. The insulating film acts as a passivation film or a layer-to-layer insulating film in multilevel interconnections.

However, there are disadvantages with the conventional method of producing semiconductor device with the Cu metallization mentioned above. That is, the oxidation temperature of Cu ranges from 200 to 250°C, whereas the heat treating temperature in the CVD is of the order of 400°C or over. Therefore, Cu in the metallization film is easily oxidized due to oxygen which exists in an ambient atmosphere when depositing the insulating film by the CVD process. Oxidation of Cu damages the surface of the metallization film which is in contact with the insulation film and therefore degrades the Cu metallization film especially in terms of its resistance.

SUMMARY OF THE INVENTION

Accordingly, a general object of the present invention is to provide a novel and useful method of producing a semiconductor device, in which the above problems have been eliminated.

A more specific object of the present invention is to provide a method of producing a semiconductor device, in which oxidation of a metallization film including at least copper is effectively prevented and its metallization resistance can be kept low even after deposition of an insulating layer.

Another object of the present invention is to provide a method of producing a semiconductor device, in which a copper interconnection of a low resistance is formed.

Still another object of the present invention is to provide a method of producing a semiconductor device, in which an electromigration is effectively suppressed.

To attain the above-mentioned objects and features, according to the present invention, there is provided a method of producing a semiconductor device comprising the steps of depositing an alloy film including copper (Cu) on a substrate, patterning the alloy film, and annealing the patterned alloy film in an ambient atmosphere including N_2, so that a copper (Cu) interconnection film covered by a nitride film is formed.

According to the present invention, a semiconductor device produced by the above method is provided. That is, a semiconductor device according to the present invention comprises a substrate, a copper interconnection film deposited on the substrate, and a nitride film covering said copper film, wherein the copper film and the nitride firm

are formed by depositing an alloy film including copper on the substrate, patterning the alloy film, and annealing the patterned alloy film in an ambient atmosphere including at least N_2.

According to the present invention, there is another method of producing a semiconductor device comprising the steps of depositing a copper interconnection film on a substrate, patterning the copper film, depositing a nitride film on the copper film and the substrate, and etching off the nitride film that is not part of the nitride film deposited on surfaces of the patterned copper film.

According to the present invention, there is another semiconductor device comprising a silicon substrate, an insulating film deposited on the silicon substrate, a barrier metal film for preventing reaction and interdiffusion between copper and silicon, deposited on the insulating film, a copper interconnection film deposited on the barrier metal film, a nitride film enclosing top and side surfaces of the copper film, and another insulating film deposited on the copper film covered by the nitride film.

Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS.1A through 1C are respectively cross sectional views for explaining an example of a method of producing a semiconductor device according to the present invention;

FIGS.2A and 2B are respectively cross sectional views for explaining steps for producing an alloy film;

FIGS.3A and 3B are respectively graphs showing experimental results for the measurement of the sheet resistivity;

FIGS.4A through 4C are respectively graphs showing experimental results for the measurement of the X-ray diffraction;

FIG.5A is a cross sectional view of an example of a semiconductor device produced by the method of the present invention;

FIG.5B is a cross sectional view along a line X-X in FIG.5A;

FIG.5C is a cross sectional view along a line Y-Y in FIG.5A; and

FIGS.6A through 6D are respectively cross sectional views for explaining another example of a method of producing a semiconductor device according to the present invention.

DETAILED DESCRIPTION

A description will first be given on a method of producing a semiconductor device which uses an alloy of copper and titanium (Cu-Ti alloy) for an interconnection film, by referring to FIGS.1A through 1C.

As shown in FIG.1A, an alloy film 14 consisting of Cu and Ti is deposited on a diffusion barrier metal film 12 which is deposited on an insulating film 10. The deposition of the Cu-Ti alloy may be carried out by a direct current (D.C.) magnetron sputtering method, in which a Cu-Ti alloy target is sputtered. The content of Ti in the Cu-Ti alloy film 14, which determines the thickness of a barrier film 16 for preventing Cu films from being oxidized, is preferably in the range from 1 to 40 weight %. The greater the content of Ti, the longer is the time required for growing the barrier film 16. The thickness of the Cu-Ti alloy film 14 preferably ranges from 3,000 Å to 2μm. The sputtering is carried out, for example, in an ambient atmosphere of argon (Ar) gas at a pressure of 5mTorr with a power of D.C.4kw.

Another method for depositing the Cu-Ti alloy film 14 may be used instead of the above method using the Cu-Ti alloy target. That is, as shown in FIG.2A, a Cu film 14a is first deposited on the diffusion barrier metal film 12 by the D.C. magnetron sputtering in which a Cu target is sputtered. Then, as shown in FIG.2B, a Ti film 14b is deposited on the top of the Cu film 14a by the D.C. magnetron sputtering in which a Ti target is sputtered. Then, the Cu/Ti bilayer deposited on the barrier film 12 is annealed at a low pressure for alloying Cu with Ti to form the Cu-Ti alloy film 14 shown in FIG.1A. This low-pressure-furnaced annealing (abbreviated as LPFA) is carried out in Ar gas at 550°C, for example. The Ar gas acts to prevent Ti from being oxidized during annealing.

The diffusion barrier metal film 12 acts to prevent Cu atoms from reacting with and diffusing into the insulating film 10 made of phosphor-silicate glass (PSG), silicon dioxide (SiO_2) or silicon nitride (Si_3N_4), for example. The diffusion barrier metal film 12 may be made of titanium nitride (TiN), tungsten (W), tungsten nitride (WN), zirconium nitride (ZrN), titanium carbide (TiC), tungsten carbide (WC), tantalum (Ta), tantalum nitride (TaN) or titanium tungsten (TiW). The thickness of the diffusion barrier metal film 12 is preferably in the range from 1,000Å to 2000Å. When using TiN to form the diffusion barrier metal film 12, for example, a reactive magnetron sputtering method may be used. The deposition of TiN is carried out in such a manner that a Ti target is sputtered in an ambient atmosphere of $Ar + N_2$ gas at a pressure of 5mTorr with a pow r of D.C.4kW, for example.

Next, the Cu-Ti alloy film 14 thus deposited is patterned in accordance with an interconnection pattern by an ion milling, as shown in FIG.1B. This ion milling process uses a SiO_2 mask or a PSG mask and is carried out in Ar gas at a pressure of 2×10^{-4}Torr with an accelerating voltage of 500V, for example. Instead of the ion milling, a reactive ion etching (abbreviated as RIE), in which $CCl_4 + Cl_2$ gas is used, may also be used for patterning.

Preferably, the diffusion barrier metal film 12 is also patterned after the patterning of the Cu-Ti alloy film 14. Since the diffusion barrier metal film 12 is provided to protect the diffusion of Cu atoms into the insulating film 10, the pattern of the diffusion barrier metal film 12 is made almost identical with the pattern of the Cu-Ti alloy film 14. The patterning of the diffusion barrier metal film 12 of TiN, for example, may be performed by the reactive ion etching method in an ambient atmosphere of SF_6 gas at a pressure of 0.02 to 0.05Torr with a power of 50 to 200W, for example.

Then, the patterned Cu-Ti alloy film 14 is annealed. The annealing is carried out in an ambient atmosphere of nitrogen (N_2) gas at a temperature of 600 to 900°C for tens of minutes to a few hours. During annealing, Ti atoms are diffused toward top and side surfaces of the patterned film 14, and combined with N_2 in the atmosphere, so that the film 16 of TiN for oxidation resistance is formed on the top and side surfaces of the patterned film 14. With the out-diffusion of Ti atoms, the Cu atoms in the Cu-Ti alloy film 14 approach a pure state, so that there is finally formed an almost pure Cu film 18 which is covered by the TiN film 16. The Cu film 18 is an excellent interconnection film, because it is almost pure and thus its resistivity is kept extremely low. The thickness of the TiN film 16 depends on the annealing time and the content of Ti in the Cu-Ti film 14. Preferably, the TiN film 16 has the thickness of 500Å to 2,000Å. The aforementioned annealing is preferably carried out at a low pressure such as 4Torr. The gas for annealing is not limited to N_2 ambients, and gases including N_2 such as $Ar + N_2$ or NH_3(ammonia)$+ N_2$ may be used.

The Cu interconnection film 18 is provided with oxidation resistance, since the top and side surfaces thereof are totally covered by the TiN film 16. In addition, since the Cu film 18 is deposited on the diffusion barrier metal film 12, the diffusion of Cu atoms into the insulating film 10 or a silicon substrate (not shown) through a contact hole (not shown) formed in the insulating film 10 is effectively prevented. As a result, even when an insulating film which acts as a layer-to-layer insulating film or a passivation film is d posited by means of the CVD at a temperature of approximately 420°C on the Cu film 18 which is covered by the TiN film 16, the oxidation of the Cu film 18 can be effectively prevented, so that the Cu interconnection layer of an extremely low resistance can be obtained. In addition, the gen ration of the electromigration in the Cu film 18 may be effectively prevented, since the Cu film 18 is formed by annealing at a high temperature in the range of 600 to 900°C. Therefore, the grain size grows larger.

A description will be given on a method of producing another semiconductor device in which a Cu interconnection film is totally covered by a barrier film of zirconium nitride (ZrN) which prevents the Cu interconnection film from being oxidized, by referring to FIGS.1A through 1C.

First, the alloy film 14 of Cu-Zr is deposited on the diffusion barrier metal layer 12. The deposition of the Cu-Zr alloy may be carried out by the D.C. magnetron sputtering method using a Cu-Zr alloy target. The content of Zr in the Cu-Zr alloy film 14, which determines the thickness of the barrier film 16 of ZrN, is preferably in the range from 1 to 40 weight %. The thickness of the Cu-Zr alloy film 14 ranges from 3,000Å to 2μm. The parameters for sputtering are the same as those when sputtering of the Cu-Ti target described.

The Cu-Zr alloy film 14 may also be formed by depositing a Cu/Zr bilayer on the diffusion barrier metal film 12 in that order and then carrying out the low-pressure annealing in N_2 gas at a temperature of 650°C, for example.

Steps following the deposition of the Cu-Zr alloy film 14 are performed in a similar way to the steps in the method of producing the Cu-Ti alloy film described previously. That is, the Cu-Zr alloy film 14 is patterned by means of the ion milling. Then, the diffusion barrier metal film 12 is etched off by the RIE. Finally, the patterned Cu-Zr alloy film 14 deposited on the patterned diffusion barrier metal film 12 is annealed, so that there is obtained the Cu film 18 totally covered by the ZrN film 16 which provides oxidation resistance for the Cu film 18.

The reason for use of Ti or Zr as explained in the foregoing is that the standard free generation energy thereof is relatively low and therefore nitride of Ti or Zr can easily be obtained. Instead of TiN or ZrN which is electrically conductive, an electrically insulating material of nitride such as BN, AlN or Si_3N_4 may be used to totally cover the top and side surfaces of the Cu interconnection film 18. A description will be given on the method of producing a semiconductor device, in which the Cu interconnection film is covered by such an insulating film, by using FIGS.1A through 1C.

As a first step, the alloy film 14 of Cu-Al, for example, is deposited on the top of the diffusion barrier metal film 12 made of TiN, TiW, W, ZrN, TiC, Ta TaN, TiW or WC by the D.C. magnetron

sputtering, in which a Cu-Al alloy target including Al of 1 to 40 weight % therein is sputtered. The sputtering is carried out in an ambient atmosphere of Ar gas at a pressure of 5mTorr with a power of D.C.4kW, for example. The thickness of the Cu-Al film 14 is preferably in the range from 5,000Å to 2μm. Next, the Cu-Al alloy film 14 is patterned by ion milling etching, as shown in FIG.1B. The etching parameters are the same as those mentioned previously. Thereafter, the diffusion barrier metal film 12 is preferably patterned by the RIE. Then, the patterned Cu-Al alloy film 14 is annealed in the atmosphere including N_2 gas at a low pressure. In detail, the annealing is carried out at a pressure of 4Torr and a temperature of 600 to 900°C for 30 to 90 minutes. During annealing, Al atoms are diffused out and then react with N_2 in the atmosphere, so that the barrier film 16 of AlN which prevents the oxidation of Cu is formed on the top and side surfaces of an almost pure Cu interconnection film 18. The thickness of the AlN barrier film 16 preferably ranges from 300Å to 1,500Å. Procedures for forming a BN or Si_3N_4 barrier film other than the AlN barrier film may be carried out in a similar way to the procedures for the AlN film.

A description will now be given of experimental results for the measurement of the sheet resistance of the interconnection film. In the experiment, two samples each having the barrier film 16 of TiN which were respectively formed by the following two different processes.

Process 1Step 1:

The Cu film 14a (FIG.2A) of the thickness of 2,000Å was formed on the TiN film 12 by the D.C. magnetron sputtering, and then the Ti film 14b of the thickness of 1,500Å was deposited on the Cu film 14a by the D.C. magnetron sputtering.

Step 2:

Next, the Cu-Ti bilayer thus formed was annealed in Ar gas at a pressure of 4Torr and a temperature of 550°C for 30 minutes in order to obtain the Cu-Ti alloy film 14.

Step 3:

Then, the Cu-Ti alloy was annealed in N_2 gas at a pressure of 4Torr and a temperature of 750°C for 30 minutes.

Process 2Step 1:

The Cu film 14a (FIG.2A) of the thickness of 2,000Å was formed on the TiN film 12 by the D.C. magnetron sputtering, and then the Ti film 14b of the thickness of 1,000Å was deposited on the Cu film 14a by the D.C. magnetron sputtering.

Step 2:

Next, the Cu-Ti bilayer thus formed was annealed in N_2 gas in a pressure of 4Torr and a temperature of 650°C for 30 minutes in order to obtain the Cu-Ti alloy film 14.

Step 3:

Then, the Cu-Ti alloy was annealed in N_2 gas at a pressure of 4Torr and a temperature of 750°C for 30 minutes.

FIG.3A shows the sheet resistance (μΩ/□) of the conductor including Cu measured for each of the steps in process 1 above, and FIG.3B shows the sheet resistance (μΩ/□) measured for each of the steps in process s above. As shown in FIGS.3A and 3B, the sheet resistance measured after step 2 in each of the processes 1 and 2 is larger than that in the as-deposited state after step 1 in each of processes 1 and 2. This is because the Cu/Ti bilayer has been alloyed by annealing. However, the sheet resistance after step 3 in each of processes 1 and 2 decreases and is close to the sheet resistance after step 1. This means that the Cu-Ti alloy has been changed into almost pure Cu due to the out-diffusion of Ti, which reacts with N_2. This is supported by the X-ray diffraction experiments, which is described below. In FIG.3A, the sheet resistance after step 3 is slightly larger than that after step 1. This is because the annealing time of 30 minutes in step 3 was not sufficient to totally diffuse the Ti atoms toward the top and side surfaces of the Cu-Ti alloy film.

FIGS.4A through 4C respectively show the experimental results of the X-ray diffraction measurement. FIG.4A shows the results regarding an as-deposited Cu/Ti bilayer formed by depositing a Cu film of the thickness of 2,000Å on the Si_3N_4 insulating film and further depositing a Ti film of a thickness of 1,000Å on the Cu film. FIG.4B shows the results regarding the Cu-Ti alloy obtained by annealing the Cu/Ti bilayer in an ambient atmosphere of Ar gas at a pressure of 4Torr and a temperature of 550°C for 30 minutes. FIG.4C shows the results regarding the Cu film covered by the TiN film obtained by ann aling the Cu-Ti alloy in N_2 gas at

a pressure of 4Torr and a temperature of 750°C for 30 minutes. In FIG.4A, a very strong spectrum of Cu, especially the spectrum of (111) can be observed, whereas spectra of Cu_3Ti, Cu_4Ti and Cu_2Ti are notable in FIG.4B. This means that Cu atoms have been alloyed with Ti atoms. Further, very strong spectra of Cu and Ti can be observed in FIG.4C. This means that the film including Cu has been changed into an almost pure state after being annealed in N_2 gas.

A description will now be given of an example of a semiconductor device having a two-level metallization obtained in accordance with the method of the present invention.

Referring to FIGS.5A through 5C, an insulating film 22 such as SiO_2 is deposited on a p-type of a Si substrate 20. The insulating film 22 is partially etched off to form a contact hole 24. On the insulating film 22 and over the contact hole 24, there are deposited a Ti film 26 of a thickness of 500Å, a TiN diffusion barrier metal film 28 of a thickness of 1,000Å and a Cu interconnection film 32 in that order. The Ti film 26 is provided to make a better ohmic contact to a n^+-diffused layer 20a formed in the Si substrate 20. The deposition of the Ti film 26 may be carried out by the D.C. magnetron sputtering in an ambient atmosphere of Ar gas at a pressure of 5mTorr with a power of 2kW, for example. The deposition of the TiN film 28, a barrier film 30 of TiN and the Cu film 32 is performed in accordance with the method of the present invention discussed in the foregoing.

On the insulating film 22 and the Cu film 32 covered by the TiN film 30, there is deposited a layer-to-layer insulating film 34 such as PSG by the CVD. Although the temperature in the CVD process is approximately 420°C, the Cu film 32 is not oxidized because of the presence of the TiN film 30 which totally covers the Cu film 32. On the layer-to-layer insulating film 34, there is deposited a TiN barrier metal film 36 and a Cu interconnection film 40 which is totally covered by a TiN barrier film 38. This deposition is carried out in accordance with the method of the present invention described in the foregoing. The ohmic contact between the Cu film 32 at the first level and the Cu film 40 at the second level is formed through a contact hole 42 formed in the insulating film 34. It should be noted that a metallic film such as the Ti film 26 is not required because the bottom of the contact hole 42 is formed with the TiN film 36.

There is deposited a passivation film 44 on the insulating film 34 and the TiN film 38 by the CVD, for example. An Al bonding pad 46 for packaging is deposited on the top of the Cu film 40 covered by the TiN film 38. Although Al is liable to react with Cu, the illustrated structure can prevent the reaction, because the Cu film 40 is totally covered by the TiN film 38.

In the structure explained above, an Al film may be used instead of the TiN film 26, and W, WN, ZrN, TiC, Wc, Ta, TaN or TiW may be used instead of the TiN film 28 or 36. The insulating film 22, 34 or 44 may be formed by Si_3N_4 instead of SiO_2 or PSG. Moreover, the barrier film 30 or 38 may be formed by ZrN, AlN, BN or Si_3N_4. When using AlN, BN or Si_3N_4 to cover the Cu film 32 or 40, it is necessary to etch off the insulating film to form the through hole.

A description will be given of another method of producing a semiconductor device in which a Cu interconnection film is covered by a barrier film for the oxidation resistance, referring to FIGS.6A through 6D.

First, referring to FIG.6A, a PSG insulating film 52 is deposited on a Si substrate 50 by the CVD, for example. SiO_2 or Si_3N_4 may also be used instead of PSG. On the top of the PSG insulating film 52, there is deposited a diffusion barrier metal film 54 of TiN by the reactive magnetron sputtering in which a Ti target is sputtered at an ambient atmosphere of $Ar + N_2$ gas at a pressure of 5mTorr with a power of D.C.4kW. The thickness thereof preferably ranges from 100Å to 1,000Å. Of course, use of W, WN, ZrN, TiC, WC, Ta, TiW or TaN other than TiN is possible. Next, a Cu interconnection film 56 is deposited on the TiN film 54 by the D.C. magnetron sputtering in which a Cu target is sputtered in an ambient atmosphere of Ar gas at a pressure of 5mTorr with a power of D.C.2kW, for example. The thickness of the Cu film 56 is preferably in the range from 3,000Å to 2μm. Then, the Cu film 56 is etched off by the ion milling method to pattern the Cu film 56. The etching is carried out in an ambient atmosphere of Ar gas at a pressure of 2×10^{-4}Torr with an accelerating voltage of 500V, for example. The mask of SiO_2 or PSG is used upon etching. Thereafter, a TiN film 58 for preventing Cu from being oxidized is deposited around the surfaces of the patterned Cu film 56 and on the TiN film 54. The deposition of the TiN film 58 may be carried out by the reactive magnetron sputtering. The sputtering is carried out in an ambient atmosphere of $Ar + N_2$ gas at a pressure of 5mTorr with a power of D.C.4kW, for example. The thickness of the TiN film 58 ranges from 1,000Å to 2,000Å.

As a next step, as shown in FIG.6B, the TiN film 54 and the TiN film 58 is etched off by the reactive ion etching (RIE) in which a mask 60 such as SiO_2 or PSG is mounted on the top of the TiN barrier film 58 under which the patterned Cu film 56 is arranged. The etching is performed in an

ambient atmosphere of SF_6 gas at a pressure of 0.02 to 0.05Torr with a power of 100 to 200W, for example. The cross sectional view of the semiconductor device after the etching is illustrated in FIG.6C. Part of the films 54 and 58 which do not face the mask 60 have been taken off. Consequently, the Cu film 56 is totally enclosed by the TiN films 54 and 58.

Further, an insulating film 62 such as PSG is deposited around the Cu film 56 totally covered by TiN as well as on the insulating film 52 by the CVD. The deposition by use of the CVD is carried out in an ambient atmosphere of 1% PH_3(50cc) + N_2(50cc) gas at a pressure of 1Torr and a temperature of 420°C. It should be appreciated that the Cu film 56 is never oxidized during the CVD process because of the presence of the TiN film 58. When forming a single-level metallization semiconductor device, the insulating film 62 acts as the passivation film, whereas the insulating film 62 acts as the layer-to-layer insulating film when the multilevel metallization is formed.

The present invention is not limited to the embodiments, but various variations and modifications may be made without departing from the scope of the present invention.

Claims

1. A method of producing a semiconductor device characterized in that said method comprises the steps of depositing an alloy film (14) including copper (Cu) on a substrate, patterning said alloy film, and annealing said patterned alloy film in an ambient atmosphere including nitrogen (N_2) gas, so that a copper interconnection film (18) covered by a nitride film (16) is formed.

2. A method of producing a semiconductor device as claimed in claim 1, characterized in that said alloy film is made of an alloy of Cu and a material selected from the group consisting of titanium (Ti), zirconium (Zr), aluminum (Al), boron (B) and silicon (Si).

3. A method of producing a semiconductor device as claimed in any of claims 1 and 2, characterized in that said step of annealing is performed at a reduced pressure.

4. A method of producing a semiconductor device as claimed in any of claims 1 to 3, characterized in that said step of annealing is performed at a temperature of 600 to 900°C.

5. A method of producing a semiconductor device as claimed in any of claims 1 to 4, characterized in that said step of annealing is performed for tens of minutes to a few hours.

6. A method of producing a semiconductor device as claimed in any of claims 1 to 5, characterized in that the thickness of said nitride film ranges from 500Å to 1,000Å.

7. A method of producing a semiconductor device as claimed in any of claims 1 to 6, characterized in that said ambient atmosphere is gas including N atoms.

8. A method of producing a semiconductor device as claimed in any of claims 1 to 6, characterized in that said ambient atmosphere is a gas including N atoms and a gas selected from the group including algon (Ar) and ammonia (NH_3).

9. A method of producing a semiconductor device as claimed in any of claims 1 to 8, characterized in that said nitride is a material selected from the group including titanium nitride (TiN), zirconium nitride (ZrN), aluminum nitride (AlN), boron nitride (BN) and silicon nitride (Si_3N_4).

10. A method of producing a semiconductor device as claimed in any of claims 1 to 9, characterized in that said substrate includes a metallic film (12) deposited on an insulating film (10) on a silicon substrate.

11. A method of producing a semiconductor device as claimed in any of claims 1 to 10, characterized in that said step of depositing said alloy film is performed by a direct current magnetron sputtering in which an alloy including Cu target is sputtered.

12. A method of producing a semiconductor device as claimed in any of claims 1 to 10, characterized in that said step of depositing said alloy is performed by depositing a bilayer film consisting of a Cu film (14a) and a metallic material (14b) which is alloyed with said Cu film on said substrate in that order and by annealing said bilayer film.

13. A method of producing a semiconductor device as claimed in any of claims 1 to 12, characterized in that the thickness of said alloy film ranges from 3,000Å to 2μm.

14. A method of producing a semiconductor device as claimed in any of claims 1 to 13, characterized in that a metallic material other than Cu is included as 1 to 20 weight % in said alloy film.

15. A method of producing a semiconductor device as claimed in any of claims 1 to 14, characterized in that said step of patterning is carried out by an ion milling method.

16. A method of producing a semiconductor device as claimed in any of claims 1 to 15, characterized in that said method further comprises a step of depositing an insulating film on said Cu interconnection film covered by said nitride.

17. A method of producing a semiconductor device as claimed in any of claims 1 to 16, characterized in that said deposition of said insulating film is carried out by a chemical vapor deposition (CVD).

18. A semiconductor device characterized in that said device comprises a substrate (10, 12); a copper interconnection film (18) deposited on said substrate; and a nitride film (16) covering said copper film, wherein said copper film and said nitride film are formed by depositing an alloy film (14) including copper on said substrate, patterning said alloy film, and annealing said patterned alloy film in an ambient atmosphere including nitrogen (N_2) gas.

19. A semiconductor device as claimed in claim 18, characterized in that said nitride film is made of a material selected from the group consisting of titanium nitride (TiN), zirconium nitride (ZrN), aluminum nitride (AlN), boron nitride (BN) and silicon nitride (Si_3N_4).

20. A semiconductor device as claimed in any of claims 18 and 19, characterized in that said substrate is made up of a silicon substrate, an insulating film (10) deposited on said silicon substrate and a diffusion barrier metal film (12) for preventing reaction and interdiffusion between copper and silicon, deposited on said insulating film.

21. A semiconductor device as claimed in any of claims 18 to 20, characterized in that said diffusion barrier metal film is made of a material selected from the group consisting of titanium nitride (TiN), tungsten (W), tungsten nitride (WN), zirconium nitride (ZrN), titanium carbide (TiC), tungsten carbide (WC), tantalum (Ta), tantalum nitride (TiN) and titanium tungsten (TiW).

22. A semiconductor device as claimed in any of claims 18 to 21, characterized in that an insulating film is deposited on said copper film covered by the nitride.

23. A method of producing a semiconductor device characterized in that said method comprises the steps of depositing a copper interconnection film (56) on a substrate (50, 52, 54); patterning said copper interconnection film; depositing a nitride film (58) on said copper film and said substrate; and etching off said nitride film that is not part of said nitride film deposited on surfaces of said patterned copper film.

24. A method of producing a semiconductor device as claimed in claim 23, characterized in that said step of depositing said copper film is carried out by a direct current magnetron sputtering method.

25. A method of producing a semiconductor device as claimed in any of claims 23 and 24, characterized in that said step of depositing said nitride film is carried out by a reactive magnetron sputtering method.

26. A method of producing a semiconductor device as claimed in any of claims 23 to 25, characterized in that said step of patterning said copper film is performed by an ion milling method.

27. A method of producing a semiconductor device as claimed in any of claims 23 to 26, characterized in that said step of etching off is performed by a reactive ion etching method.

28. A semiconductor device characterized in that said device comprises a silicon substrate (50); an insulating film (52) deposited on said silicon substrate; a barrier metal film (54) for preventing reaction and interdiffusion between copper and silicon, deposited on said insulating film; a copper interconnection film (56) deposited on said barrier metal film; a nitride film (58) covering top and side surfaces of said copper film; and another insulating film (62) deposited on said copper film covered by said nitride film.

29. A semiconductor device as claimed in claim 28, characterized in that said nitride film is made of a material selected from the group consisting of titanium nitride (TiN), zirconium nitride (ZrN), aluminum nitride (AlN), boron nitride (BN) and silicon nitride (Si_3N_4).

FIG. 1A

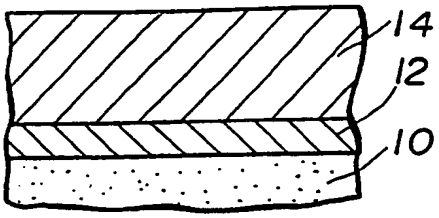


FIG. 1B

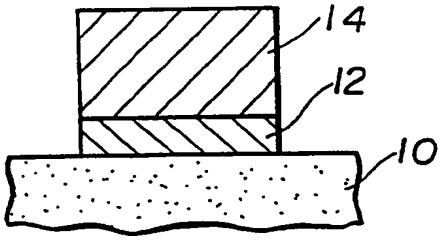


FIG. 1C

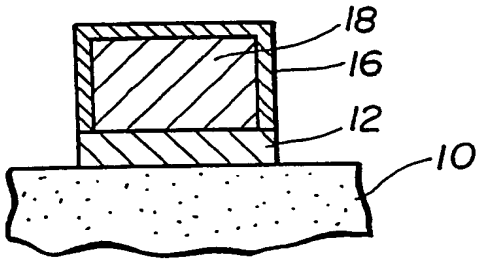


FIG. 2A

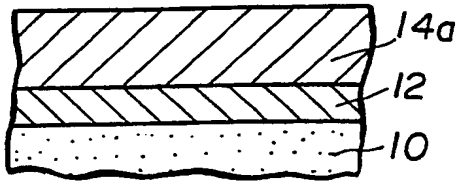


FIG. 2B

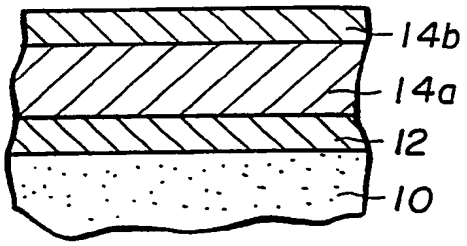


FIG. 3A

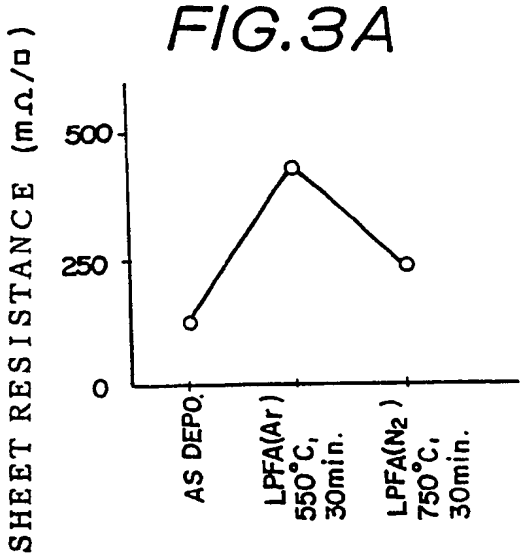


FIG. 3B

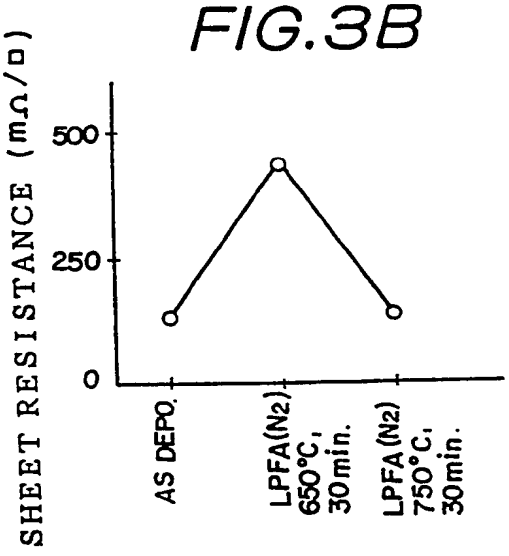


FIG.4A

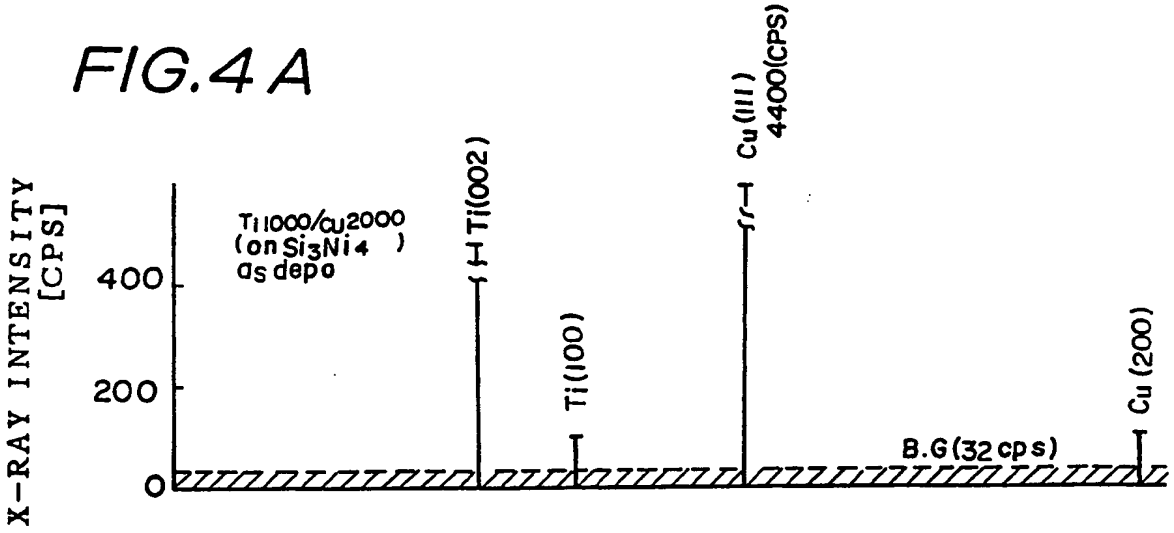


FIG.4B

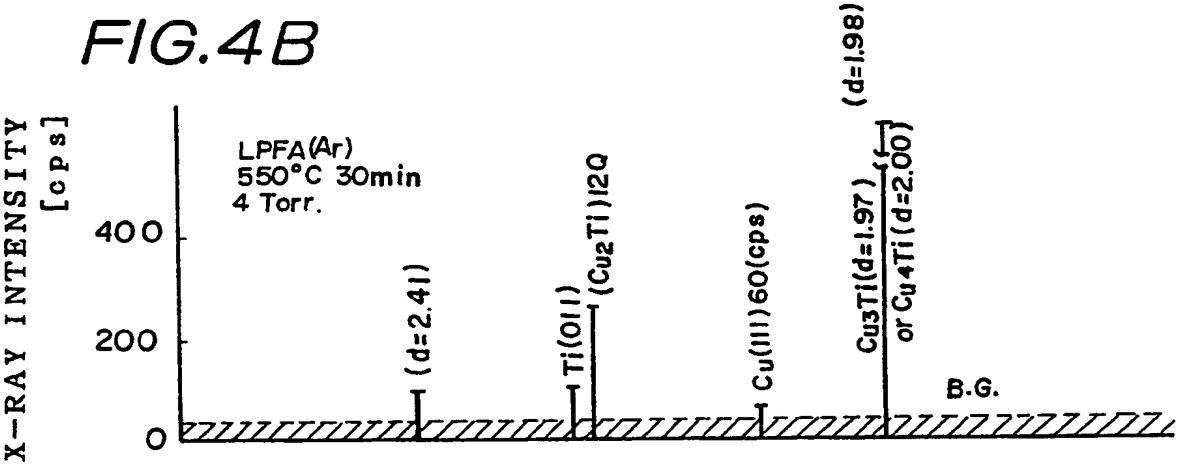
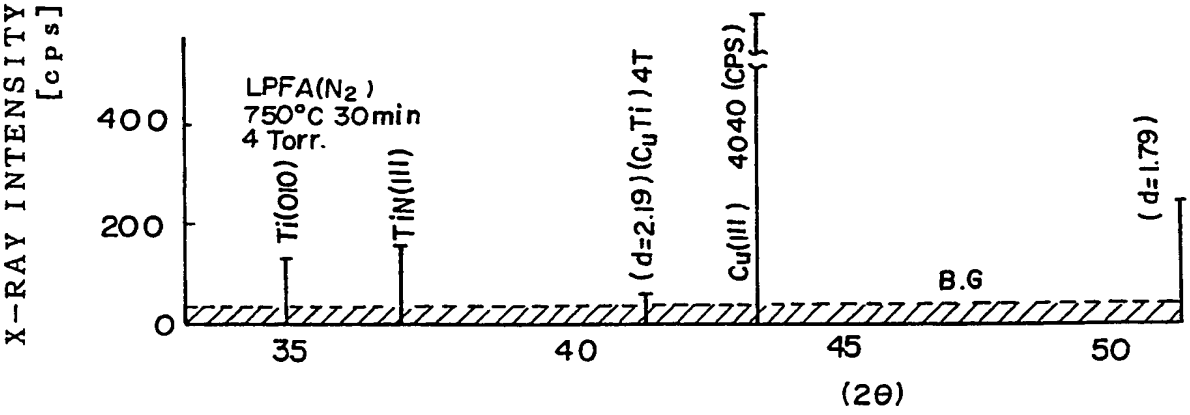


FIG.4C



DIFFRACTION ANGLE (°)

FIG.5A

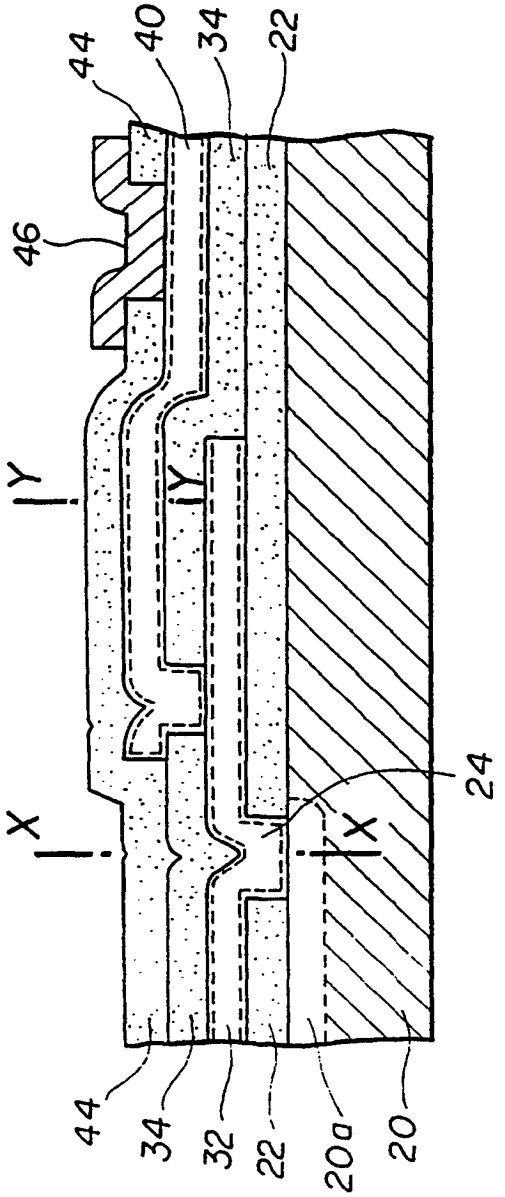


FIG.5C

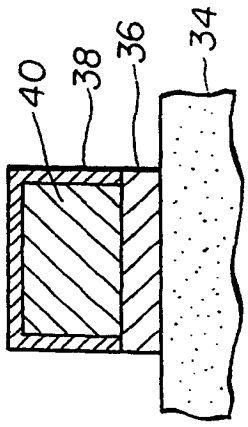


FIG.5B

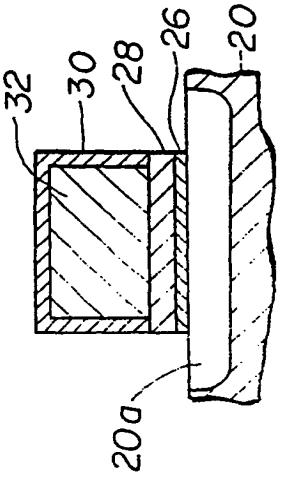


FIG.6A

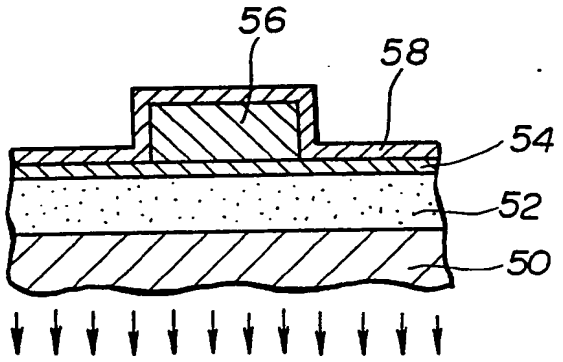


FIG.6B

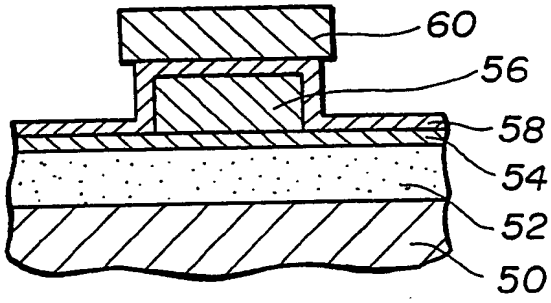


FIG.6C

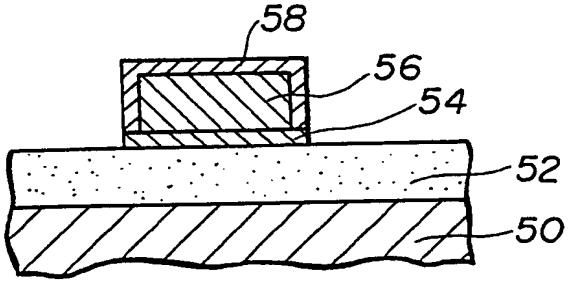
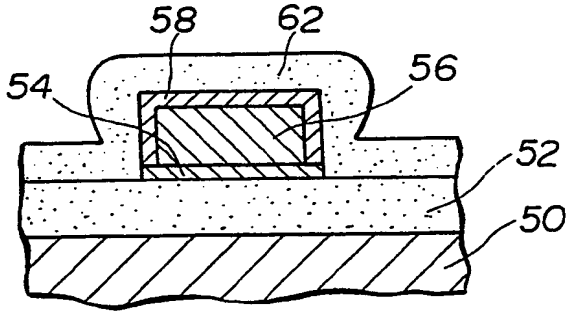


FIG.6D



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(54) Method of producing semiconductor device and semiconductor device.

(57) A method of producing a semiconductor device comprising the steps of depositing an alloy film (14) including copper (Cu) on a substrate (10,12), patterning the alloy film, and annealing the patterned alloy film in an ambient atmosphere including at least nitrogen (N_2) gas, so that a copper interconnection film (18) covered by a nitride film (16) is formed.

FIG. 1A

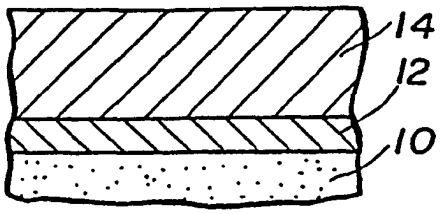


FIG. 1B

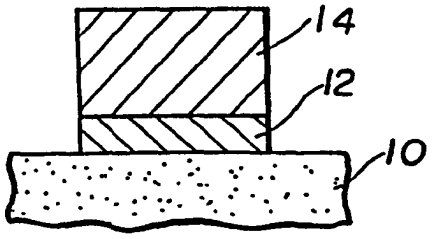
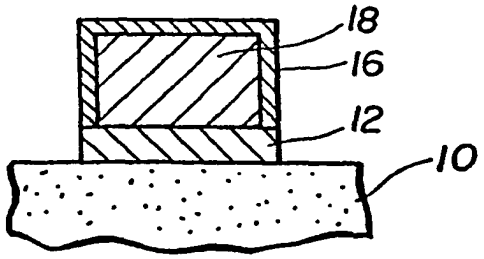


FIG. 1C



EP 0 260 906 A3

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EUROPEAN SEARCH REPORT

Application Number

EP 87 30 8090

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	JP-A-53 116 089 (HITACHI) * Figure 2 * ---	1,18,23,28	H 01 L 21/90 H 01 L 21/318 H 01 L 23/52
A	THIN SOLID FILMS, vol. 69, no. 1, June 1980, pages 379-386, Elsevier Sequoia, Lausanne, CH; R.J. MILLER et al.: "Electromigration in gold and copper thin film conductors" * Page 380, paragraphs 2-4 * ---	1,18,23,28	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 15, no. 4, September 1972, page 1088, New York, US; J.E. ORDONEZ: "Protective coatings against corrosion in metal electrodes" ---		
A	US-A-4 429 011 (KIM et al.) -----		
			TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10-10-1988	PHEASANT N.J.

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